

DATA SHEET

BLV857

UHF linear push-pull power
transistor

Product specification
Supersedes data of 1995 Oct 04

1997 Jan 16

UHF linear push-pull power transistor

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FEATURES

- Internal input matching for an optimum wideband capability and high gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATION

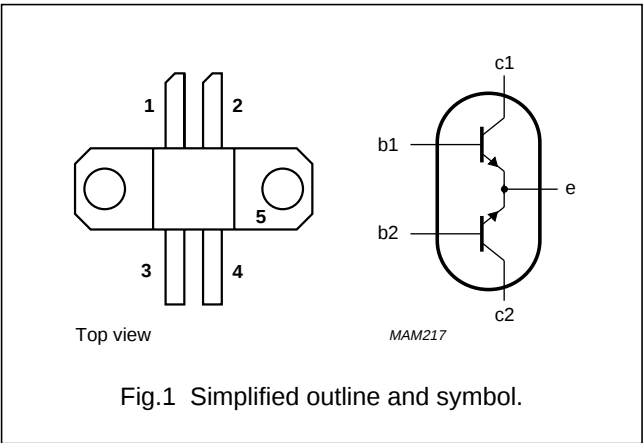
- Common emitter class-A operation in linear transposers/transmitters (television) in the 470 to 860 MHz frequency band.

DESCRIPTION

NPN silicon planar transistor with two sections in push-pull configuration. The device is encapsulated in a SOT324B 4-lead rectangular flange package with a ceramic cap. The common emitters are connected to the flange.

PINNING SOT324B

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1
2	c2	collector 2
3	b1	base 1
4	b2	base 2
5	e	common emitters



QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ }^{\circ}\text{C}$ in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\text{ sync}}$ (W)	G_p (dB)
CW class-A	860	25	2×1.1	$\geq 10^{(1)}$	$\geq 10^{(1)}$

Note

1. Three-tone test signal (–8, –16 and –10 dB); $d_{im} = -54\text{ dB}$.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

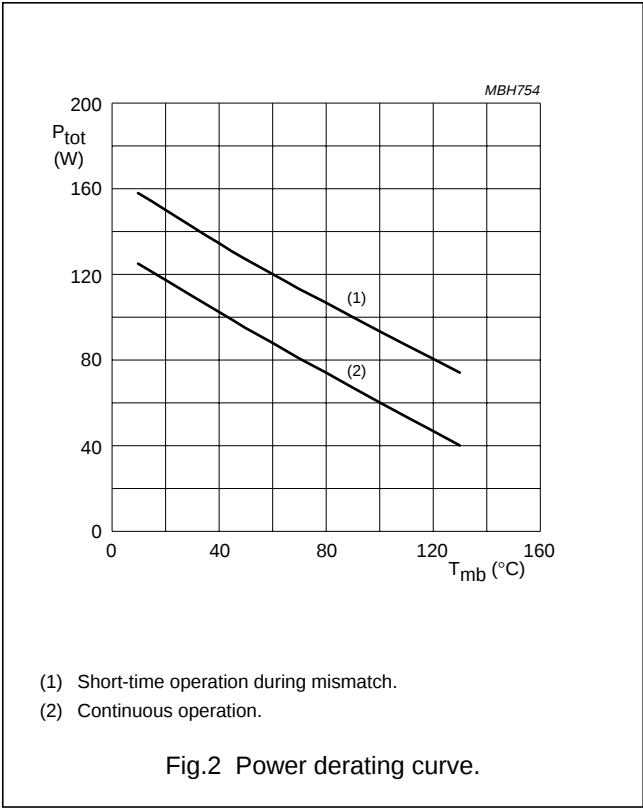
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	60	V
V _{CEO}	collector-emitter voltage	open base	–	28	V
V _{EBO}	emitter-base voltage	open collector	–	2.5	V
I _C	collector current (DC)		–	7.4	A
I _{C(AV)}	average collector current		–	7.4	A
P _{tot}	total power dissipation	T _{mb} = 70 °C; note 1; see Fig.2	–	80	W
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-mb}	thermal resistance from junction to mounting-base	P _{tot} = 80 W; T _{mb} = 70 °C note 1	1.6	K/W
R _{th mb-h}	thermal resistance from mounting-base to heatsink	note 1	0.4	K/W

Note to Limiting values and Thermal characteristics

1. Total device; both sections equally loaded.



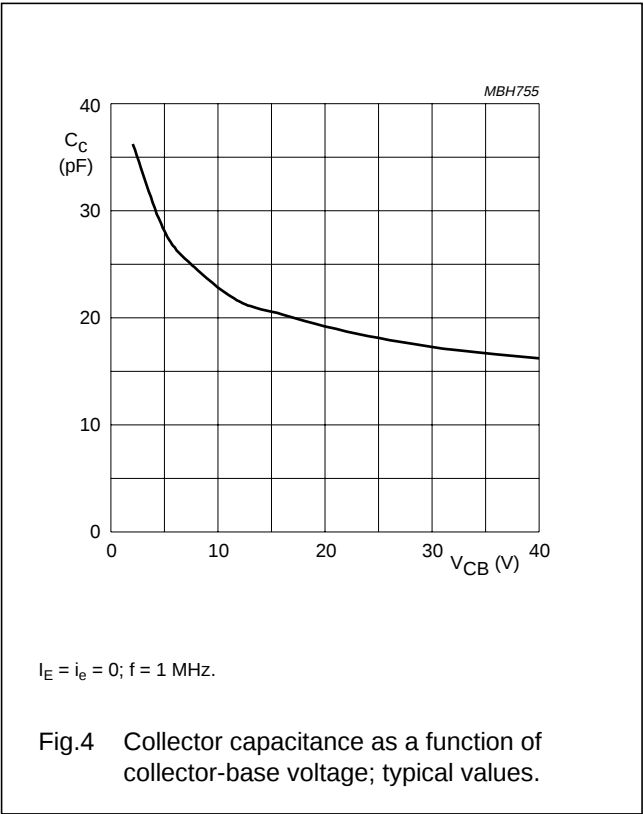
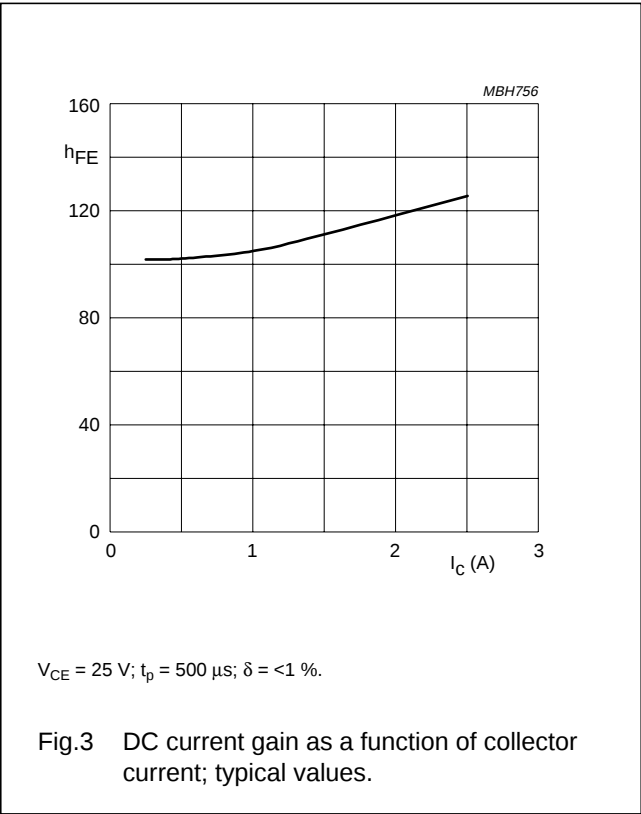
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CHARACTERISTICS

Values apply to either transistor section; $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 15\text{ mA}; I_E = 0$	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 30\text{ mA}; I_B = 0$	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	$I_E = 0.6\text{ mA}; I_C = 0$	2.5	–	–	V
I_{CBO}	collector-base leakage current	$V_{CB} = 27\text{ V}; V_{BE} = 0$	–	–	1.5	mA
I_{CEO}	collector-emitter leakage current	$V_{CE} = 20\text{ V}$	–	–	3	mA
h_{FE}	DC current gain	$V_{CE} = 25\text{ V}; I_C = 1.1\text{ A};$ see Fig.3	30	–	140	
C_c	collector capacitance	$V_{CB} = 25\text{ V}; I_E = i_e = 0; f = 1\text{ MHz};$ see Fig.4	–	18	–	pF
C_{re}	feedback capacitance	$V_{CE} = 25\text{ V}; I_C = 0; f = 1\text{ MHz}$	–	11	–	pF



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APPLICATION INFORMATION

RF performance at $T_h = 25\text{ }^{\circ}\text{C}$ in a common emitter push-pull class-A test circuit.

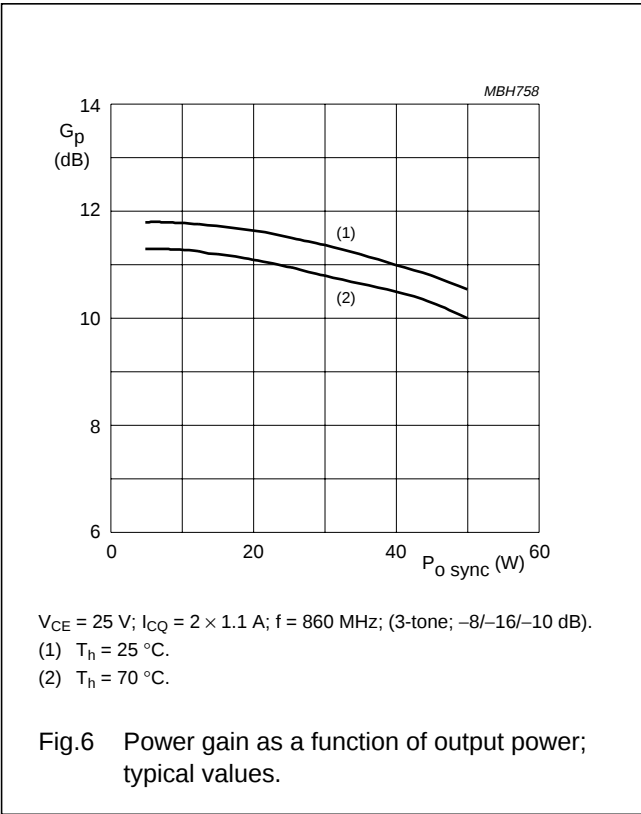
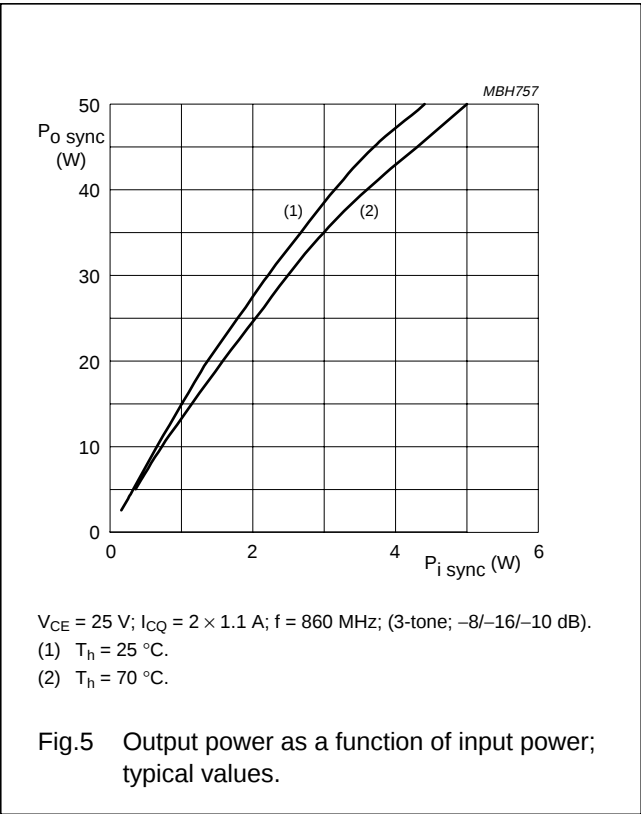
MODE OF OPERATION	f (MHz)	V _{CE} (V)	I _{CQ} (A)	P _{o sync} (W)	G _p (dB)	d _{im} (dB)
CW class-A	860	25	2 × 1.1	≥10 ⁽¹⁾	≥10 ⁽¹⁾	≤−54 ⁽¹⁾
CW class-A	860	25	2 × 1.1	≥10 ⁽²⁾	≥10 ⁽²⁾	≤−51 ⁽²⁾

Notes

- 1. Three-tone test method: $f_{\text{vision}} = 855.25\text{ MHz}$ (vision carrier −8 dB); $f_{\text{sound}} = 860.75\text{ MHz}$ (sound carrier −10 dB); $f_{\text{sideband}} = 859.68\text{ MHz}$ (sideband signal −16 dB); 0 dB corresponds to peak sync level.
- 2. Three-tone test method: $f_{\text{vision}} = 855.25\text{ MHz}$ (vision carrier −8 dB); $f_{\text{sound}} = 860.75\text{ MHz}$ (sound carrier −7 dB); $f_{\text{sideband}} = 859.68\text{ MHz}$ (sideband signal −16 dB); 0 dB corresponds to peak sync level.

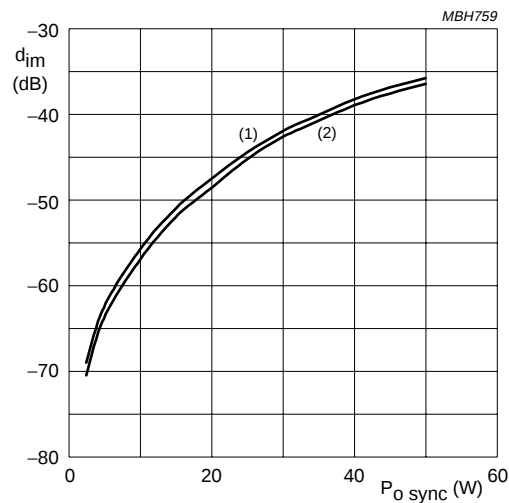
Ruggedness in class-A operation

The BLV857 is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the conditions: $V_{\text{CE}} = 25\text{ V}$; $I_{\text{CQ}} = 2 \times 1.1\text{ A}$; $f = 860\text{ MHz}$; $T_h = 25\text{ }^{\circ}\text{C}$; $P_{\text{o sync}} = 10\text{ W}$.



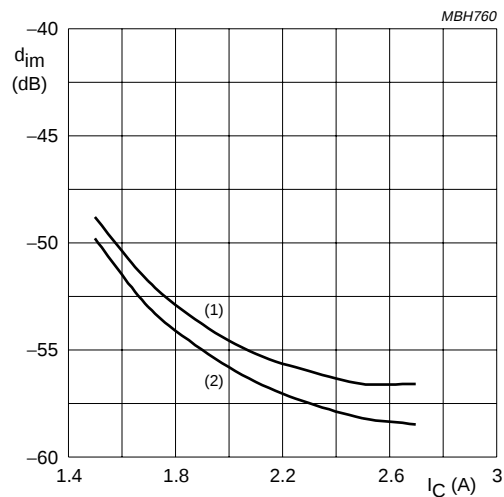
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$V_{CE} = 25\text{ V}$; $I_{CQ} = 2 \times 1.1\text{ A}$; $f = 860\text{ MHz}$; (3-tone; -8/-16/-10 dB).
(1) $T_h = 70^\circ\text{C}$.
(2) $T_h = 25^\circ\text{C}$.

Fig.7 Intermodulation distortion as a function of output power; typical values.



$V_{CE} = 25\text{ V}$; $f = 860\text{ MHz}$; (3-tone; -8/-16/-10 dB).
(1) $T_h = 70^\circ\text{C}$.
(2) $T_h = 25^\circ\text{C}$.

Fig.8 Intermodulation distortion as a function of collector current; typical values.

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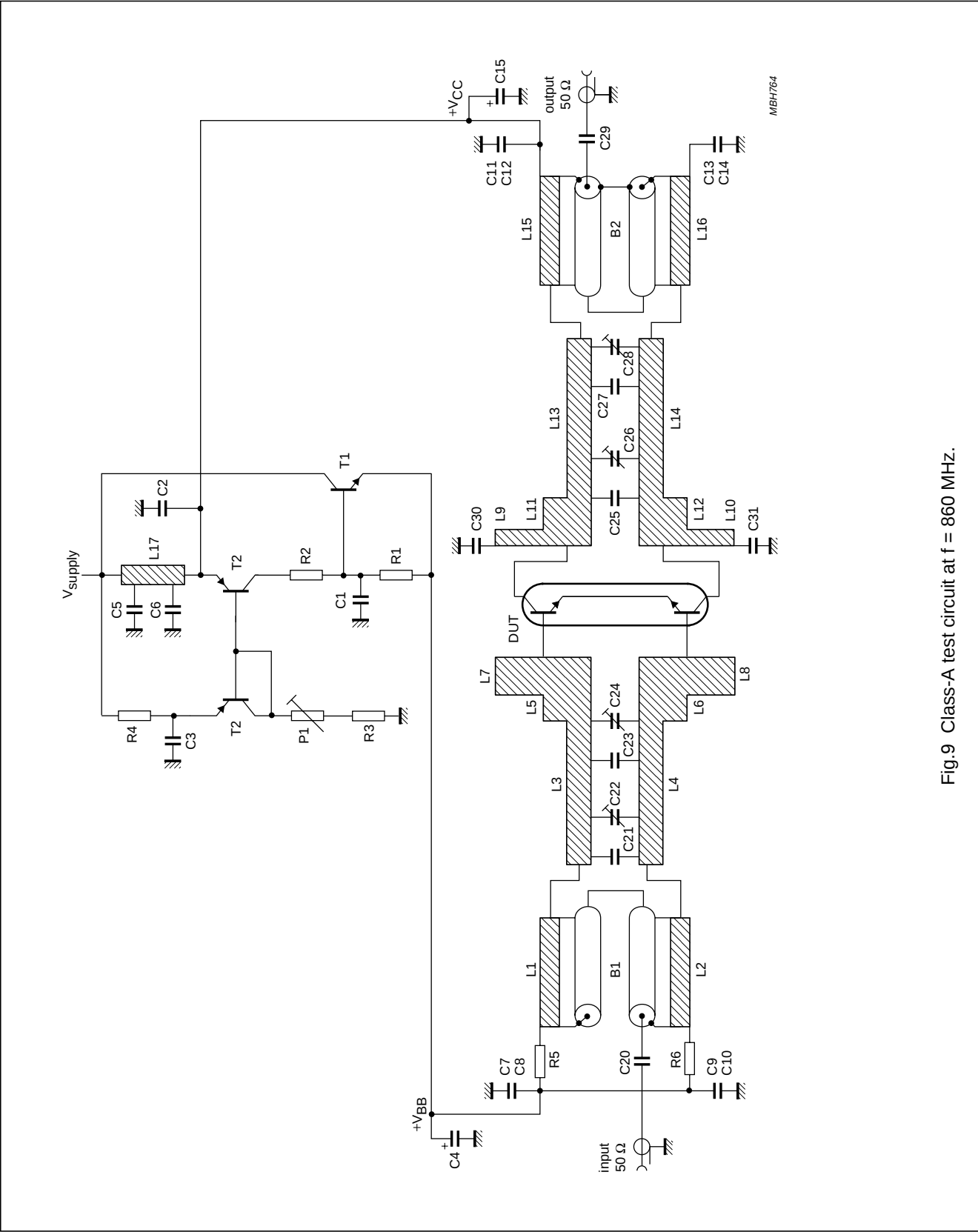
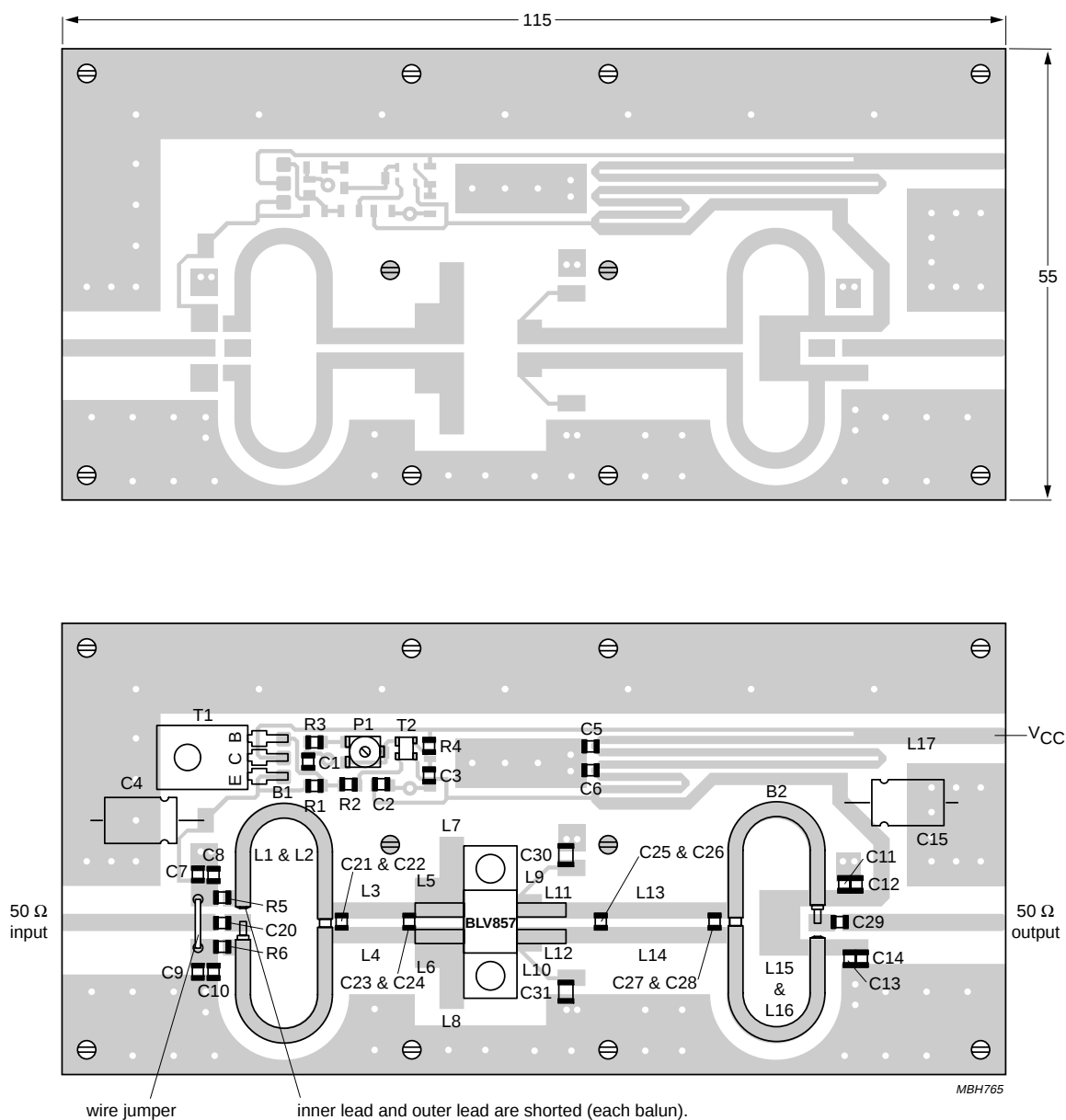


Fig.9 Class-A test circuit at f = 860 MHz.

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List of components

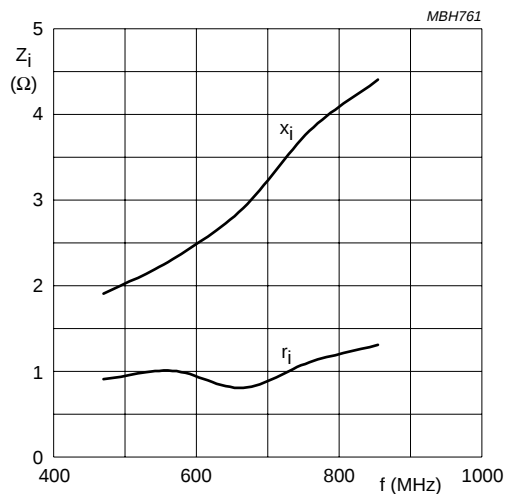
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C3, C5, C6, C7, C8, C9, C10	multilayer ceramic chip capacitor	10 nF	805	2222 590 16627
C4	solid aluminium capacitor	47 μ F; 25 V		2222 030 36479
C11, C12, C13, C14, C30, C31	multilayer ceramic chip capacitor	100 nF	1206	2222 591 16641
C15	solid aluminium capacitor	10 μ F; 63 V		2222 030 38109
C20	multilayer ceramic chip capacitor; note 1	18 pF		
C21	multilayer ceramic chip capacitor; note 1	3 pF		
C22, C24, C26, C28	Tekelec Giga trim 37271; note 3	0.6 to 4.5 pF		
C23	multilayer ceramic chip capacitor; note 1	7.5 pF		
C25	multilayer ceramic chip capacitor; notes 1 and 3	11 pF		
C27	multilayer ceramic chip capacitor; notes 1 and 3	9.1 pF		
C29	multilayer ceramic chip capacitor; note 1	100 pF		
L1, L2, L15, L16	stripline; note 2	50 Ω	30.6 $\times$ 2 mm	
L3, L4	stripline; note 2	50 Ω	10 $\times$ 2 mm	
L5, L6	stripline; note 2	26.5 Ω	3 $\times$ 5 mm	
L7, L8	stripline; note 2	15 Ω	3 $\times$ 10 mm	
L9, L10	stripline; note 2	104 Ω	6 $\times$ 0.5 mm	
L11, L12	stripline; note 2	38.8 Ω	3 $\times$ 3 mm	
L13, L14	stripline; note 2	50 Ω	22.5 $\times$ 2 mm	
L17	stripline; notes 2 and 4	76.2 Ω	120 $\times$ 1 mm	
B1, B2	Semi rigid coax balun UT70-25	$Z = 25 \Omega \pm 1.5 \Omega$	70 mm	
R1	SMD resistor	220 Ω	805	2322 734 22201
R2	SMD resistor	1.8 Ω	805	2322 734 21808
R3	SMD resistor	4.3 k Ω	805	2322 734 24302
R4	SMD resistor	33 Ω	805	2322 734 23309
R5, R6	SMD resistor	3.3 Ω	805	2322 734 23308
P1	potentiometer	2 k Ω		
T1	NPN transistor	BD139		9330 912 20112
T2	double PNP transistor	BCV62		5322 130 60505

Notes

- American Technical Ceramics type 100A or capacitor of same quality.
- The striplines are on a double copper-clad printed-circuit board: Rogers ULTRALAM 2000 (B0300M1046QB) ($\epsilon_r = 2.55$); thickness 0.76 mm.
- Position of C25 and C26: distance of centre capacitor to transistor BLV857 = 7.5 mm.
Position of C27 and C28: distance of centre capacitor to balun B2 = 1.5 mm.
- The sense resistor on the bias unit is implemented as a stripline L17, in this way we obtain a small sense resistor (approximately 80 m Ω) which can handle the dissipated power.

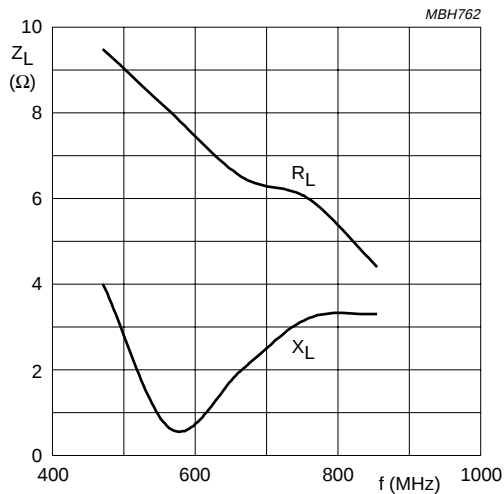
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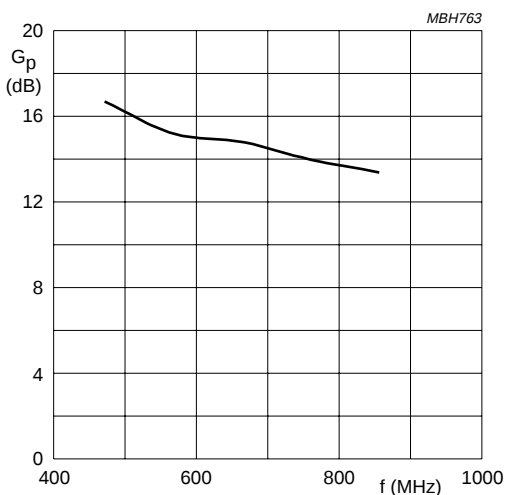
$V_{CE} = 25\text{ V}$; $I_{CQ} = 2 \times 1.1\text{ A}$; $P_{O\text{ sync}} = 10\text{ W}$ (total device); $T_h = 25\text{ }^\circ\text{C}$.

Fig.11 Input impedance (per section) as a function of frequency (series components); typical values.



$V_{CE} = 25\text{ V}$; $I_{CQ} = 2 \times 1.1\text{ A}$; $P_{O\text{ sync}} = 10\text{ W}$ (total device); $T_h = 25\text{ }^\circ\text{C}$.

Fig.12 Load impedance (per section) as a function of frequency (series components); typical values.



$V_{CE} = 25\text{ V}$; $I_{CQ} = 2 \times 1.1\text{ A}$; $P_{O\text{ sync}} = 10\text{ W}$ (total device); $T_h = 25\text{ }^\circ\text{C}$.

Fig.13 Gain as a function of frequency; typical values.

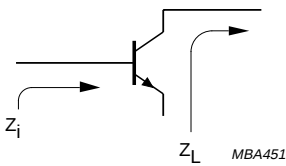
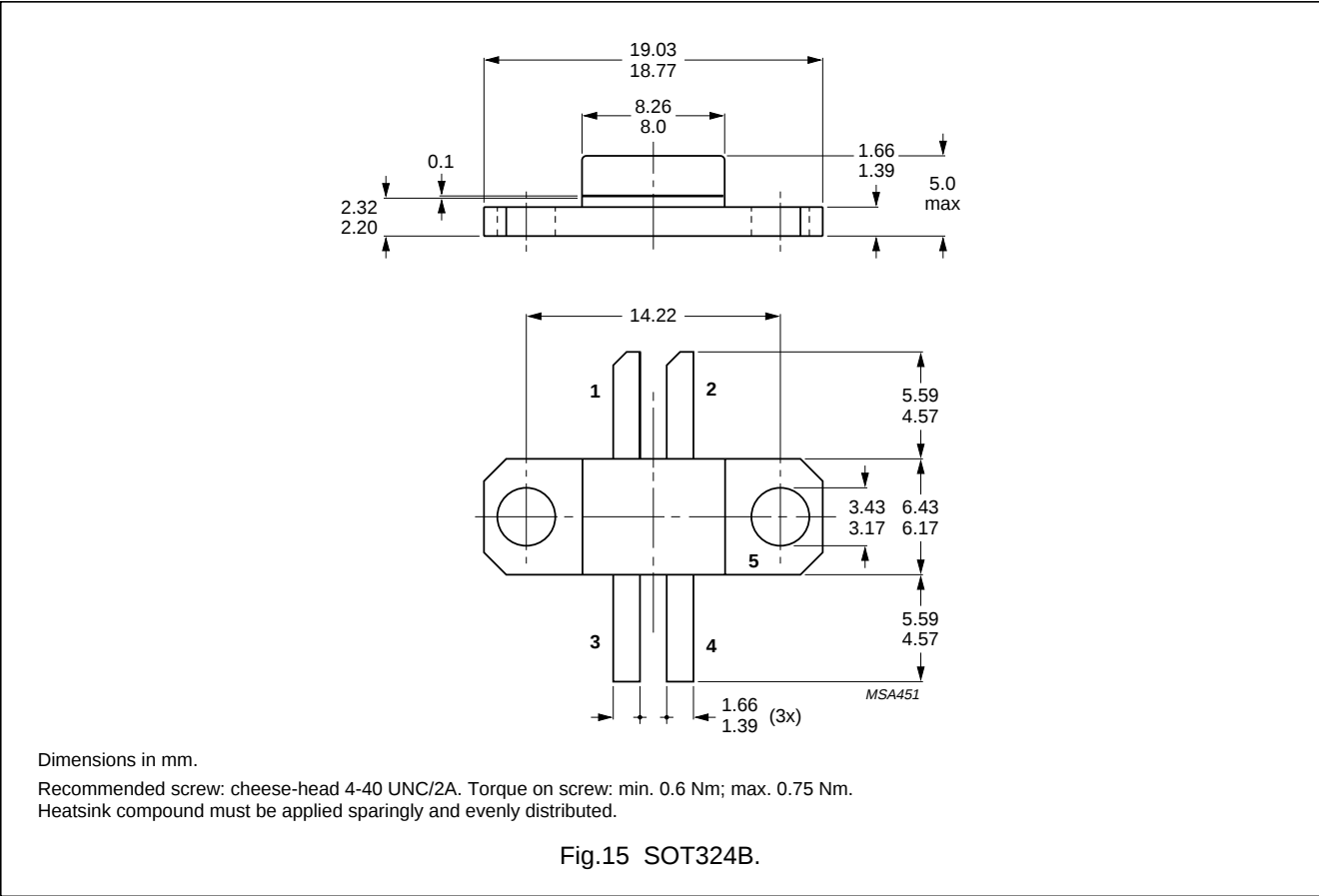


Fig.14 Definition of transistor impedance.

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PACKAGE OUTLINE



DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

127067/0/02/pp12

Date of release: 1997 Jan 16

Document order number: 9397 750 01381

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